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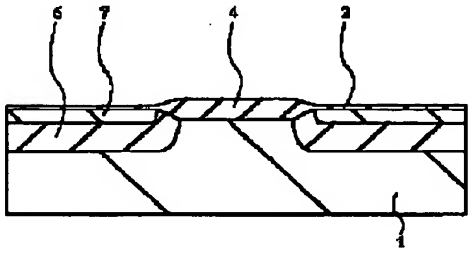
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

(57) Abstract:

PURPOSE: To provide a semiconductor device having element separating areas which can improve the operating speed and degree of integration of a semiconductor integrated circuit device.

CONSTITUTION: Since single-crystal silicon layers 7 for forming semiconductor elements are surrounded by element separating areas which are formed in a LOCOS oxide film 4 formed on the main surface of a silicon substrate and composed of buried oxide films 6, completely depleted semiconductor elements can be formed and, in addition, highly flat narrow element forming areas can be formed on the main surface of the substrate 1.



* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] It is semiconductor integrated circuit equipment which embeds, is constituted by the oxide film and characterized by the thing which are semiconductor integrated circuit equipment which has the isolation region between components which surrounds each active region in which a semiconductor device is formed, by which the isolation region between said components was formed in the interior of the LOCOS oxide film formed on the principal plane of a semi-conductor substrate, and said semi-conductor substrate, and for which said LOCOS oxide film set caudad, and said embedding oxide film bent in the direction of a front face of said semi-conductor substrate, and is connected with said LOCOS oxide film.
[Claim 2] The manufacture approach of the semiconductor integrated circuit equipment characterized by being the manufacture approach of semiconductor integrated circuit equipment according to claim 1, forming a LOCOS oxide film on the principal plane of a semi-conductor substrate, embedding by heat-treating and forming an oxide film after driving oxygen ion into said semi-conductor substrate with the energy which does not penetrate said LOCOS oxide film.
[Claim 3] The manufacture approach of the semiconductor integrated circuit equipment characterized by to embed by heat-treating, to form an oxide film, and subsequently to the principal plane top of said semi-conductor substrate to form a LOCOS oxide film after being the manufacture approach of semiconductor integrated circuit equipment according to claim 1, forming a trapezoid photoresist mask on the principal plane of a semi-conductor substrate, driving in oxygen ion to said semi-conductor substrate with the energy which does not penetrate said photoresist mask and removing said photoresist mask.
[Claim 4] The isolation region between said components which is semiconductor integrated circuit equipment which has the isolation region between components which surrounds each active region in which a semiconductor device is formed, and is formed in the principal plane top of a semi-conductor substrate and the interior is semiconductor integrated circuit equipment characterized by being constituted with the embedding oxide film.
[Claim 5] Semiconductor integrated circuit equipment characterized by said embedding oxide film which is semiconductor integrated circuit equipment according to claim 4, and adjoins touching in the front face of said semi-conductor substrate.
[Claim 6] The manufacture approach of the semiconductor integrated circuit equipment characterized by being the manufacture approach of semiconductor integrated circuit equipment according to claim 4 or 5, forming a trapezoid photoresist mask on the principal plane of a semi-conductor substrate, removing said photoresist mask, embedding by heat-treating subsequently, and forming an oxide film after driving in oxygen ion to said semi-conductor substrate with the energy which does not penetrate said photoresist mask.
[Claim 7] It is the manufacture approach of the semiconductor integrated circuit equipment which is the manufacture approach of semiconductor integrated circuit equipment according to claim 2, 3, or 6, and is characterized by for the placing energy of said oxygen ion being 100 - 200keV, and the amount of placing being 1017-1018cm-2.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention is applied to the semiconductor integrated circuit equipment which has the isolation region between components which separates the semiconductor device of each other electrically about semiconductor integrated circuit equipment and its manufacture approach, and relates to an effective technique.
[0002]
[Description of the Prior Art] SOI (Silicon on Insulator) in which it embedded on the silicon single crystal and the silicon film was formed through the oxide film can realize the improvement of resistance to reduction of the parasitic capacitance of a semiconductor device, and a radiation, a latch rise free-lancer's complementary MOS FET (Metal Oxide Semiconductor Field Effect Transistor;CMOSFET), etc.
[0003] As indicated by No. 63, No. 11, and P.1088 in "application physics [furthermore,]" 1994 in SOI By embedding with the field oxide formed on the principal plane of the silicon film, and connecting an oxide film Each active region in which a semiconductor device is formed can be completely surrounded with an oxide film, it can dissociate electrically, and the perfect depletion mold semiconductor device from which high mobility and a big drive current are acquired can be obtained by depletion-izing this active region by the depletion mode.
[0004] According to the place which this invention person examined, the following two approaches can mainly be considered as an approach of forming the isolation region between components which surrounds completely the active region where a semiconductor device is formed in SOI.
[0005] namely, RIE (Reactive Ion Etching) -- until it reaches an embedding oxide film by law -- the silicon film of the surface layer of SOI -- the slot where width of face is narrow -- **** -- subsequently The ****** separation method which aims at separation between components by embedding this slot with an insulating material, And the LOCOS (Local Oxidation of Silicon) oxide film formed of the **** oxidation which uses a nitride as a mask is formed on the principal plane of the silicon film of the surface layer of SOI. It is the **** oxidation separation method which aims at separation between components by forming thickly until it embeds this LOCOS oxide film and reaches an oxide film.
[0006]
[Problem(s) to be Solved by the Invention] However, to the above-mentioned approach of forming the isolation region between components in SOI, this invention person found out that there were the following troubles.
[0007] That is, in the above-mentioned ****** separation method, formation of a slot and the embedding process of a slot are complicated, and since a routing counter increases further, there is a problem that a manufacturing cost increases.
[0008] Moreover, although the formation process of a LOCOS oxide film is easy, in order that the breadth (BAZU beak) to the longitudinal direction of a LOCOS oxide film may progress, it is not suitable [separation method / the surface smoothness of the front face of the silicon film of SOI worsens and] for high integration further, as the above-mentioned **** oxidation separation method thickens thickness of a LOCOS oxide film.
[0009] The purpose of this invention is to offer the semi-conductor substrate which has the isolation region between components which can realize improvement in the speed and high integration of semiconductor integrated circuit equipment.

[0010] Other purposes of this invention are to offer the technique in which an easy production process can attain the above-mentioned purpose.
[0011] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0012]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application. That is, the semiconductor integrated circuit equipment of (1) this invention has the isolation region between components which surrounds each active region in which a semiconductor device is formed, the isolation region between said components is constituted by the embedding oxide film formed in the interior of the LOCOS oxide film formed on the principal plane of a semi-conductor substrate, and said semi-conductor substrate, and said LOCOS oxide film set caudad, and said embedding oxide film bent in the direction of a front face of said semi-conductor substrate, and is connected with said LOCOS oxide film.
[0013] (2) Moreover, the manufacture approach of the semiconductor integrated circuit equipment of this invention forms a LOCOS oxide film on the principal plane of a semi-conductor substrate, and after it drives oxygen ion into said semi-conductor substrate with the energy which does not penetrate said LOCOS oxide film, embed it by heat-treating and it forms an oxide film.
[0014] (3) Moreover, the semiconductor integrated circuit equipment of this invention has the isolation region between components which surrounds each active region in which a semiconductor device is formed, and the isolation region between said components formed in the principal plane top of a semi-conductor substrate and the interior is constituted by the embedding oxide film.
[0015] (4) Moreover, the manufacture approach of the semiconductor integrated circuit equipment of this invention forms a trapezoid photoresist mask on the principal plane of a semi-conductor substrate, after it drives in oxygen ion to said semi-conductor substrate with the energy which does not penetrate said photoresist mask, it removes said photoresist mask, subsequently embeds it by heat-treating, and forms an oxide film.
[0016]
[Function] According to the above-mentioned means (1) and (2), in the edge of a LOCOS oxide film, in order to form an embedding oxide film, the depth of the oxygen ion driven in to a semi-conductor substrate bends in the direction of a front face from the interior of a semi-conductor substrate depending on the thickness of a LOCOS oxide film. Therefore, the isolation region between components which was formed in the interior of the LOCOS oxide film formed on the principal plane of a semi-conductor substrate and a semi-conductor substrate and which it embeds, and an oxide film is connected and surrounds an active region completely can be formed.
[0017] Furthermore, since an embedding oxide film is formed even in the lower part of the LOCOS oxide film formed on the principal plane of a semi-conductor substrate and an embedding oxide film and a LOCOS oxide film are connected, it is not necessary to thicken thickness of a LOCOS oxide film. Therefore, the level difference of the front face of a semi-conductor substrate becomes low, and a BAZU beak becomes short, and surface smoothness can form in the front face of a semi-conductor substrate the good isolation region between components where width of face is narrow.
[0018] Moreover, according to the above-mentioned means (3) and (4), in the edge of a trapezoid photoresist mask, in order to form an embedding oxide film, depending on the thickness of a photoresist mask, the depth of the oxygen ion driven in to a semi-conductor substrate bends in the direction of a front face from the interior of a semi-conductor substrate, and arrives at even the front face of a semi-conductor substrate. Therefore, it applies and embeds on a front face from the interior of a semi-conductor substrate, an oxide film is formed, and the component isolation region which surrounds an active region completely can be formed.
[0019] Furthermore, since it embeds in the front face of a semi-conductor substrate and an isolation region between components except an oxide film is not formed, it is flat and the isolation region between components where width of face is narrow can be formed in the front face of a semi-conductor substrate.
[0020] Moreover, since according to the above-mentioned means the isolation region between components which surrounds an active region completely by driving oxygen ion into a semi-conductor substrate can be formed after forming a LOCOS oxide film or a photoresist mask, a production process can be simplified compared with the conventional technique which forms in SOI the isolation region between components

which surrounds an active region.
[0021]
[Example] Hereafter, the example of this invention is explained to a detail based on a drawing.
[0022] In addition, what has the same function in the complete diagram for explaining an example attaches the same sign, and explanation of the repeat is omitted.
[0023] (Example 1) The important section sectional view of the semi-conductor substrate which shows the structure of the isolation region between components which is one example of this invention to drawing 3 is shown.
[0024] The single-crystal-silicon layer 7 in which each semiconductor device is formed is surrounded, the oxide film is formed, and this oxide film is constituted by the embedding oxide film 6 formed in the interior of the LOCOS oxide film 4 formed on the principal plane of a silicon substrate 1, and a silicon substrate 1. Furthermore, the edge of the LOCOS oxide film 4 set caudad, and the embedding oxide film 6 bent in the direction of a front face of a silicon substrate 1, and is connected with the LOCOS oxide film 4.
[0025] Next, an example of the manufacture approach of the isolation region between components shown in drawing 3 is explained using drawing 1 - drawing 3 .
[0026] first, it is shown in drawing 1 -- as -- the front face of a silicon substrate 1 -- thermal oxidation processing -- the silicon oxide film 2 -- forming -- subsequently -- a silicon nitride film 3 -- CVD (Chemical Vapor Deposition) -- it deposits on a silicon substrate 1 in law.
[0027] Next, the photoresist 5 formed on the silicon substrate 1 is used as a mask, and the silicon nitride film 3 located in the field which forms the LOCOS oxide film 4 on the principal plane of a silicon substrate 1 behind is etched.
[0028] Next, after removing a photoresist 5, as shown in drawing 2 , the LOCOS oxide film 4 with a thickness of about 0.3 micrometers is formed by performing **** oxidation. Next, after removing a silicon nitride film 3, in order to embed at a silicon substrate 1 and to form an oxide film 6, oxygen ion is driven in with the energy which does not penetrate the LOCOS oxide film 4, for example, 100-200KeV, 1017-1018cm-2 all over a silicon substrate 1.
[0029] Then, as elevated-temperature annealing 1100 degrees C or more is performed in Ar ambient atmosphere for about 6 hours, the surface layer of the silicon substrate 1 which was amorphous by high energy and high concentration ion implantation is made to recrystallize for example, and it is shown in drawing 3 , it is about 0.1-1.0 micrometers to the surface layer of a silicon substrate 1. The single-crystal-silicon layer 7 is formed and about 0.4-micrometer embedding oxide film 6 is formed in coincidence.
[0030] Under the present circumstances, since oxygen ion is driven in with the energy which does not penetrate the LOCOS oxide film 4, the embedding oxide film 6 is not formed under the LOCOS oxide film 4. However, in the edge of the LOCOS oxide film 4, since the thickness of the LOCOS oxide film 4 becomes thin, oxygen ion is driven in to a silicon substrate 1. Therefore, the isolation region between components which embeds with the LOCOS oxide film 4, an oxide film 6 is connected, embeds with the LOCOS oxide film 4, and consists of oxide films 6 is formed.
[0031] According to this example, it can surround by the isolation region between components which embeds each active region in which a semiconductor device is formed with the LOCOS oxide film 4, and consists of an oxide film 6, and can insulate completely electrically. Moreover, since it is not necessary to thicken thickness of the LOCOS oxide film 4, the narrow isolation region between components of width of face with sufficient surface smoothness can be formed in the front face of a silicon substrate 1.
[0032] (Example 2) Next, the isolation region between components which is one example of this invention, and its manufacture approach are explained using drawing 4 -6.
[0033] The isolation region between components of this example is constituted by the embedding oxide film 6 which surrounded the single-crystal-silicon layer 7 in which each semiconductor device field is formed as shown in drawing 5 or drawing 6 .
[0034] The isolation region between components of this example is formed of the process shown in drawing 4 - drawing 6 .
[0035] First, as shown in drawing 4 , the silicon oxide film 2 is formed in the front face of a silicon substrate 1 by thermal oxidation processing, and, subsequently the mask by the trapezoid photoresist 8 is formed in the location which needs the isolation region between components of the front face of a silicon substrate 1.
[0036] Next, oxygen ion is driven in with the energy which does not penetrate a photoresist 8, for example, 100-200KeV, 1017-1018cm-2 all over a silicon substrate 1 like the manufacture approach indicated in the

example 1. Then, as elevated-temperature annealing 1100 degrees C or more is performed in Ar ambient atmosphere for about 6 hours and it is shown in drawing 5 after removing a photoresist 8 for example, it is about 0.1-1.0 micrometers to the surface layer of a silicon substrate 1. The single-crystal-silicon layer 7 is formed and it is about 0.4 micrometers to coincidence. The embedding oxide film 6 is formed. Under the present circumstances, since oxygen ion is driven in with the energy which does not penetrate a photoresist 8, the embedding oxide film 6 is not formed under the photoresist 8. However, since the configuration of a photoresist 8 is a trapezoid, in the edge of a photoresist 8, oxygen ion is driven in to a silicon substrate 1, and the formed embedding oxide film 6 bends in the direction of a front face from the interior of a silicon substrate 1, and arrives at even the front face of a silicon substrate 1.

[0037] In addition, in order to make the electric insulation of each active region perfect, the dimension of a photoresist 8 may be shortened, and as shown in drawing 6 , the adjoining embedding oxide film 6 may be connected.

[0038] According to this example, it can surround by the isolation region between components which embeds each active region in which a semiconductor device is formed, and consists of an oxide film 6, and can insulate completely electrically. Moreover, since the LOCOS oxide film 4 is not used together, it is flat in the front face of a silicon substrate 1, and the isolation region between components where width of face is narrow can be formed in it.

[0039] (Example 3) Next, the isolation region between components which is one example of this invention, and its manufacture approach are explained using drawing 7 and drawing 8 .

[0040] As shown in drawing 8 , the isolation region between components of this example is constituted by the LOCOS oxide film 4 and the embedding oxide film 6, and the edge of the LOCOS oxide film 4 set it caudad, and the embedding oxide film 6 turned at it in the direction of a front face of a silicon substrate 1, and it is connected with the LOCOS oxide film 4. However, the edge of the LOCOS oxide film 4 is not formed in the single-crystal-silicon layer 7 which is an active region, but is formed in the outside of the embedding oxide film 6 which surrounds the single-crystal-silicon layer 7.

[0041] First, as shown in drawing 4 , after driving in oxygen ion by using the trapezoid photoresist 8 as a mask with the energy which does not penetrate a photoresist 8 all over a silicon substrate 1, then removing a photoresist 8 like the manufacture approach indicated in the example 2, the embedding oxide film 6 which surrounds each single-crystal-silicon layer 7 is formed by performing elevated-temperature annealing.

[0042] Next, as shown in drawing 7 , after depositing a silicon nitride film 3 with a CVD method on a silicon substrate 1, a photoresist 5 is used as a mask and the silicon nitride film 3 located between the adjoining single-crystal-silicon layers 7 which were surrounded with the embedding oxide film 6 is etched. Next, after removing a photoresist 5, as shown in drawing 8 , the LOCOS oxide film 4 is formed by performing **** oxidation.

[0043] According to this example, it can surround by the isolation region between components which embeds each active region in which a semiconductor device is formed with the LOCOS oxide film 4, and consists of an oxide film 6, and can insulate completely electrically. Moreover, since the edge of the LOCOS oxide film 4 is not formed in an active region, property degradation of the semiconductor device by the leakage current produced at the edge of the LOCOS oxide film 4 can be prevented.

[0044] As mentioned above, although invention made by this invention person was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which this invention is not limited to said example and does not deviate from the summary.

[0045]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated by this application is explained briefly.

[0046] Since according to this invention each active region in which a semiconductor device is formed is surrounded in the isolation region between components and it can dissociate completely electrically, a perfect depletion mold semiconductor device can be formed and improvement in the speed of semiconductor integrated circuit equipment can be enabled. Moreover, since surface smoothness can form the good isolation region between components where width of face is narrow on the principal plane of a semi-conductor substrate, micro processing becomes easy and high integration of semiconductor integrated circuit equipment can be enabled.

[0047] Furthermore, the above-mentioned isolation region between components can be formed by the easy production process which drives in oxygen ion to a semi-conductor substrate by using a LOCOS oxide film

or a photoresist as a mask.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which is one example of this invention is shown.
[Drawing 2] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which is one example of this invention is shown.
[Drawing 3] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which is one example of this invention is shown.
[Drawing 4] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which are other examples of this invention is shown.
[Drawing 5] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which are other examples of this invention is shown.
[Drawing 6] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which are other examples of this invention is shown.
[Drawing 7] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which are other examples of this invention is shown.
[Drawing 8] It is the important section sectional view of the semi-conductor substrate in which the isolation region between components which are other examples of this invention is shown.
[Description of Notations]
1 Silicon Substrate
2 Silicon Oxide Film
3 Silicon Nitride Film
4 LOCOS Oxide Film
5 Photoresist
6 Embedding Oxide Film
7 Single-Crystal-Silicon Layer
8 Photoresist

[Translation done.]

* NOTICES *

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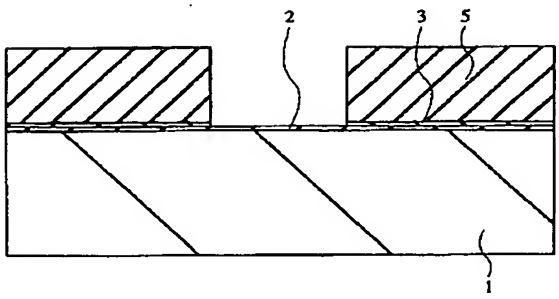
3.In the drawings, any words are not translated.

DRAWINGS

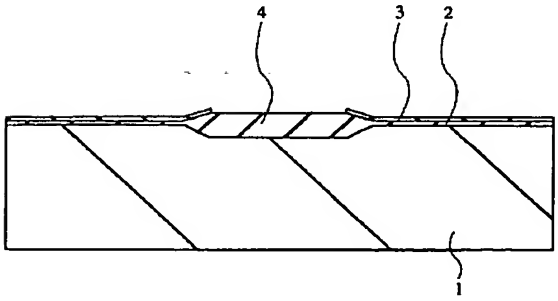
[Drawing 1]

図 1



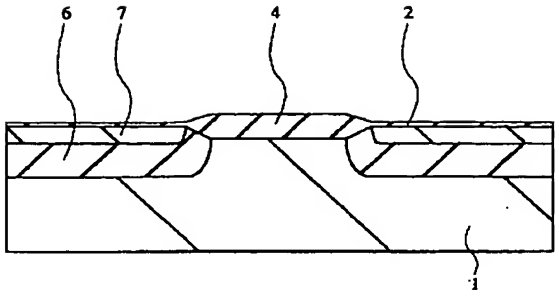
[Drawing 2]

図 2



[Drawing 3]

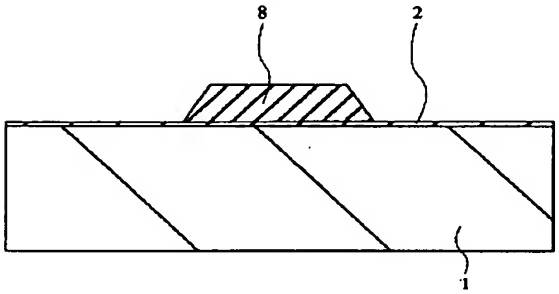
図　3



2：酸化シリコン膜
4：ＬＯＣＯＳ酸化膜
6：埋め込み酸化膜
7：単結晶シリコン層

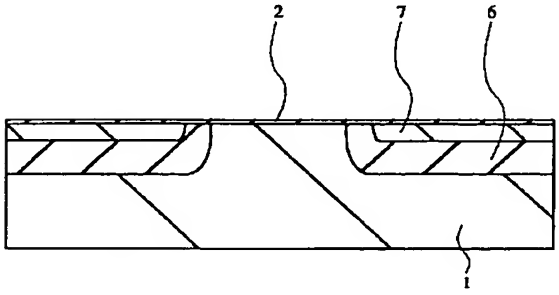
[Drawing 4]

図　4



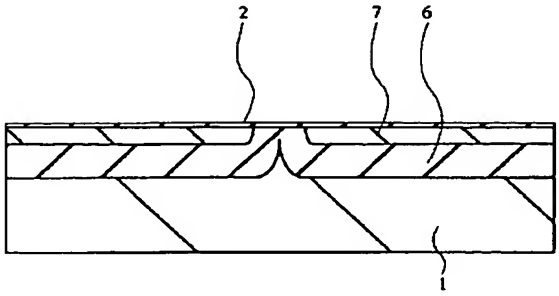
[Drawing 5]

図　5



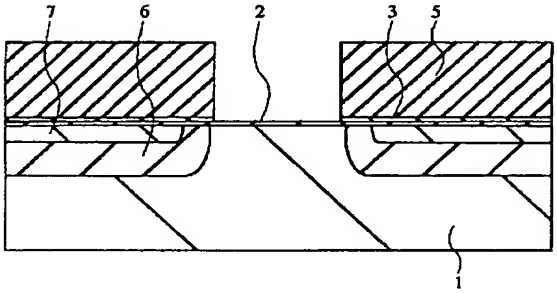
[Drawing 6]

図 6



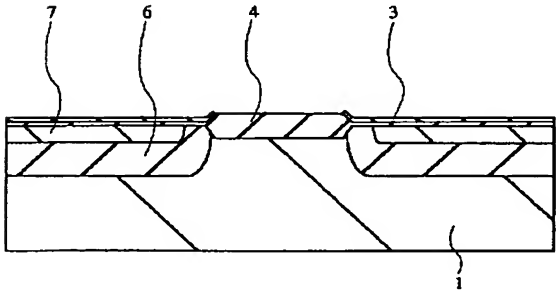
[Drawing 7]

図 7



[Drawing 8]

図 8



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	21/316				21/265	Ｊ	
	27/08	３３１			21/94	Ａ	

審査請求　未請求　請求項の数７　ＯＬ　（全７頁）

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最終頁に続く

(54)【発明の名称】　半導体集積回路装置およびその製造方法

(57)【要約】

【目的】　半導体集積回路装置の高速化および高集積化が実現できる素子間分離領域を有する半導体基板を提供する。

【構成】　シリコン基板１の主面上に形成されたＬＯＣＯＳ酸化膜４のおよび埋め込み酸化膜６からなる素子間分離領域によって、半導体素子が形成される単結晶シリコン層７が包囲されているので、完全空乏型半導体素子が形成でき、さらに、平坦性が良く幅の狭い素子間分離領域をシリコン基板１の主面上に形成することができる。

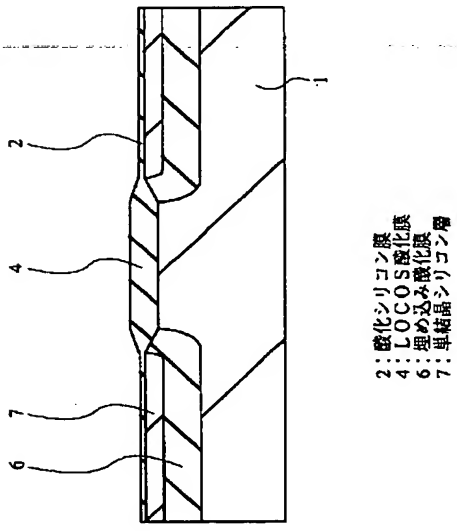


図３

【特許請求の範囲】

【請求項１】　半導体素子が形成される個々の活性領域を包囲する素子間分離領域を有する半導体集積回路装置であって、前記素子間分離領域は、半導体基板の主面上に形成されたＬＯＣＯＳ酸化膜および前記半導体基板の内部に形成された埋め込み酸化膜によって構成されており、前記埋め込み酸化膜が前記ＬＯＣＯＳ酸化膜の下方において前記半導体基板の表面方向へ曲がり、前記ＬＯＣＯＳ酸化膜とつながっていることを特徴とする半導体集積回路装置。

【請求項２】　請求項１記載の半導体集積回路装置の製造方法であって、半導体基板の主面上にＬＯＣＯＳ酸化膜を形成し、前記ＬＯＣＯＳ酸化膜を貫通しないエネルギーで酸素イオンを前記半導体基板に打ち込んだ後に、熱処理を行なうことによって埋め込み酸化膜を形成することを特徴とする半導体集積回路装置の製造方法。

【請求項３】　請求項１記載の半導体集積回路装置の製造方法であって、半導体基板の主面上に台形のホトレジストマスクを形成し、前記ホトレジストマスクを貫通しないエネルギーで酸素イオンを前記半導体基板へ打ち込み、前記ホトレジストマスクを除去した後に、熱処理を行なうことによって埋め込み酸化膜を形成し、次いで、前記半導体基板の主面上にＬＯＣＯＳ酸化膜を形成することを特徴とする半導体集積回路装置の製造方法。

【請求項４】　半導体素子が形成される個々の活性領域を包囲する素子間分離領域を有する半導体集積回路装置であって、半導体基板の主面上および内部に形成される前記素子間分離領域は、埋め込み酸化膜によって構成されていることを特徴とする半導体集積回路装置。

【請求項５】　請求項４記載の半導体集積回路装置であって、隣接する前記埋め込み酸化膜が前記半導体基板の表面において接触していることを特徴とする半導体集積回路装置。

【請求項６】　請求項４または５記載の半導体集積回路装置の製造方法であって、半導体基板の主面上に台形のホトレジストマスクを形成し、前記ホトレジストマスクを貫通しないエネルギーで酸素イオンを前記半導体基板へ打ち込んだ後に、前記ホトレジストマスクを除去し、次いで、熱処理を行なうことによって埋め込み酸化膜を形成することを特徴とする半導体集積回路装置の製造方法。

【請求項７】　請求項２、３または６記載の半導体集積回路装置の製造方法であって、前記酸素イオンの打ち込みエネルギーは、１００～２００ｋｅＶ、打ち込み量は10^{17}～$10^{18}$$cm^{-2}$であることを特徴とする半導体集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体集積回路装置およびその製造方法に関し、特に、半導体素子を互いに電気的に分離する素子間分離領域を有する半導体集積回路装置に適用して有効な技術に関するものである。

【０００２】

【従来の技術】シリコン単結晶上に埋め込み酸化膜を介してシリコン膜が形成されたＳＯＩ（Silicon on Insulator）は、半導体素子の寄生容量の低減、放射線に対する耐性の向上、およびラッチアップフリーの相補型ＭＯＳＦＥＴ（Metal Oxide Semiconductor Field Effect Transistor ；ＣＭＯＳＦＥＴ）などを実現することができる。

【０００３】さらに、例えば、「応用物理」１９９４年、第６３号、第１１号、Ｐ．１０８８に記載されているように、ＳＯＩでは、シリコン膜の主面上に形成されるフィールド酸化膜と埋め込み酸化膜をつなげることによって、半導体素子が形成される個々の活性領域を酸化膜で完全に包囲して、電気的に分離し、この活性領域をデプレッションモードで空乏化することにより、高い移動度と大きな駆動電流が得られる完全空乏型半導体素子を得ることができる。

【０００４】本発明者が検討したところによれば、ＳＯＩに、半導体素子が形成される活性領域を完全に包囲する素子間分離領域を形成する方法として、主に以下の２つの方法が考えられる。

【０００５】すなわち、ＲＩＥ（Reactive Ion Etching）法によって、埋め込み酸化膜に達するまでＳＯＩの表面層のシリコン膜に幅の狭い溝を堀り、次いで、絶縁物でこの溝を埋め込むことにより素子間分離を図る溝掘り分離法、および窒化膜をマスクとする選択酸化によって形成されるＬＯＣＯＳ（Local Oxidation of Silicon）酸化膜をＳＯＩの表面層のシリコン膜の主面上に形成し、このＬＯＣＯＳ酸化膜を埋め込み酸化膜に達するまで厚く形成することにより素子間分離を図る選択酸化分離法である。

【０００６】

【発明が解決しようとする課題】しかしながら、ＳＯＩに素子間分離領域を形成する上記方法には、以下の問題点があることを本発明者は見い出した。

【０００７】すなわち、上記溝掘り分離法では、溝の形成および溝の埋め込み工程が複雑であり、さらに工程数が多くなるため、製造コストが増大するという問題がある。

【０００８】また、上記選択酸化分離法は、ＬＯＣＯＳ酸化膜の形成工程は簡単ではあるが、ＬＯＣＯＳ酸化膜の膜厚を厚くするに従い、ＳＯＩのシリコン膜の表面の平坦性が悪くなり、さらに、ＬＯＣＯＳ酸化膜の横方向への広がり（バーズビーク）が進むため、高集積化には適していない。

【０００９】本発明の目的は、半導体集積回路装置の高速化および高集積化が実現できる素子間分離領域を有する半導体基板を提供することにある。

【００１０】本発明の他の目的は、簡単な製造工程によって上記目的を達成することのできる技術を提供することにある。

【００１１】本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【００１２】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、次のとおりである。すなわち、

（１）本発明の半導体集積回路装置は、半導体素子が形成される個々の活性領域を包囲する素子間分離領域を有しており、前記素子間分離領域は、半導体基板の主面上に形成されたＬＯＣＯＳ酸化膜および前記半導体基板の内部に形成された埋め込み酸化膜によって構成されており、前記埋め込み酸化膜が前記ＬＯＣＯＳ酸化膜の下方において前記半導体基板の表面方向へ曲がり、前記ＬＯＣＯＳ酸化膜とつながっている。

【００１３】（２）また、本発明の半導体集積回路装置の製造方法は、半導体基板の主面上にＬＯＣＯＳ酸化膜を形成し、前記ＬＯＣＯＳ酸化膜を貫通しないエネルギーで酸素イオンを前記半導体基板に打ち込んだ後に、熱処理を行なうことによって埋め込み酸化膜を形成するものである。

【００１４】（３）また、本発明の半導体集積回路装置は、半導体素子が形成される個々の活性領域を包囲する素子間分離領域を有しており、半導体基板の主面上および内部に形成される前記素子間分離領域は、埋め込み酸化膜によって構成されている。

【００１５】（４）また、本発明の半導体集積回路装置の製造方法は、半導体基板の主面上に台形のホトレジストマスクを形成し、前記ホトレジストマスクを貫通しないエネルギーで酸素イオンを前記半導体基板へ打ち込んだ後に、前記ホトレジストマスクを除去し、次いで、熱処理を行なうことによって埋め込み酸化膜を形成するものである。

【００１６】

【作用】上記した手段（１）および（２）によれば、ＬＯＣＯＳ酸化膜の端部においては、埋め込み酸化膜を形成するために半導体基板へ打ち込まれる酸素イオンの深さが、ＬＯＣＯＳ酸化膜の膜厚に依存して、半導体基板の内部から表面方向へ曲がる。従って、半導体基板の主面上に形成されたＬＯＣＯＳ酸化膜と半導体基板の内部に形成された埋め込み酸化膜がつながり、活性領域を完全に包囲する素子間分離領域を形成することができる。

【００１７】さらに、埋め込み酸化膜が、半導体基板の主面上に形成されるＬＯＣＯＳ酸化膜の下部にまで形成されて、埋め込み酸化膜とＬＯＣＯＳ酸化膜がつながるので、ＬＯＣＯＳ酸化膜の膜厚を厚くする必要がない。従って、半導体基板の表面の段差は低くなり、また、バーズビークが短くなって、平坦性が良く幅の狭い素子間分離領域を半導体基板の表面に形成することができる。

【００１８】また、上記した手段（３）および（４）によれば、台形のホトレジストマスクの端部においては、埋め込み酸化膜を形成するために半導体基板へ打ち込まれる酸素イオンの深さが、ホトレジストマスクの膜厚に依存して、半導体基板の内部から表面方向へ曲がり、半導体基板の表面にまで達する。従って、半導体基板の内部から表面にかけて埋め込み酸化膜が形成されて、活性領域を完全に包囲する素子分離領域を形成することができる。

【００１９】さらに、半導体基板の表面には埋め込み酸化膜以外の素子間分離領域は形成されないので、平坦で幅の狭い素子間分離領域を半導体基板の表面に形成することができる。

【００２０】また、上記した手段によれば、ＬＯＣＯＳ酸化膜またはホトレジストマスクを形成した後に、酸素イオンを半導体基板に打ち込むことにより、活性領域を完全に包囲する素子間分離領域を形成することができるので、活性領域を包囲する素子間分離領域をＳＯＩに形成する従来技術と比べて、製造工程を簡略化することができる。

【００２１】

【実施例】以下、本発明の実施例を図面に基づいて詳細に説明する。

【００２２】なお、実施例を説明するための全図において同一機能を有するものは同一の符号を付し、その繰り返しの説明は省略する。

【００２３】（実施例１）図３に、本発明の一実施例である素子間分離領域の構造を示す半導体基板の要部断面図を示す。

【００２４】個々の半導体素子が形成される単結晶シリコン層７を包囲して酸化膜が形成されており、この酸化膜は、シリコン基板１の主面上に形成されたＬＯＣＯＳ酸化膜４およびシリコン基板１の内部に形成された埋め込み酸化膜６によって構成されている。さらに、埋め込み酸化膜６がＬＯＣＯＳ酸化膜４の端部の下方においてシリコン基板１の表面方向へ曲がり、ＬＯＣＯＳ酸化膜４とつながっている。

【００２５】次に、図３に示した素子間分離領域の製造方法の一例を図１～図３を用いて説明する。

【００２６】まず、図１に示すように、シリコン基板１の表面に熱酸化処理により酸化シリコン膜２を形成し、次いで、窒化シリコン膜３をＣＶＤ（Chemical Vapor Deposition）法でシリコン基板１上に堆積する。

【００２７】次に、シリコン基板１上に形成されたホトレジスト５をマスクにして、後にシリコン基板１の主面上にＬＯＣＯＳ酸化膜４を形成する領域に位置する窒化シリコン膜３をエッチングする。

【００２８】次に、ホトレジスト５を除去した後、図２

に示すように、選択酸化を行なうことにより、約0.３μmの厚さのＬＯＣＯＳ酸化膜４が形成される。次に、窒化シリコン膜３を除去した後、シリコン基板１に埋め込み酸化膜６を形成するため、シリコン基板１の全面に、ＬＯＣＯＳ酸化膜４を貫通しないエネルギー、例えば、１００～２００ＫｅＶで、酸素イオンを10^{17}～$10^{18}$$cm^{-2}$打ち込む。

【００２９】続いて、例えば、Ａｒ雰囲気中で１１００℃以上の高温アニールを約６時間行ない、高エネルギー、高濃度イオン打ち込みによりアモルファス状態となったシリコン基板１の表面層を再結晶化させて、図３に示すように、シリコン基板１の表面層に約0.１～1.０μmの単結晶シリコン層７を形成し、同時に、約0.４μmの埋め込み酸化膜６を形成する。

【００３０】この際、ＬＯＣＯＳ酸化膜４を貫通しないエネルギーで酸素イオンを打ち込んでいるので、ＬＯＣＯＳ酸化膜４の下方には、埋め込み酸化膜６は形成されない。しかし、ＬＯＣＯＳ酸化膜４の端部においては、ＬＯＣＯＳ酸化膜４の膜厚が薄くなるため、酸素イオンがシリコン基板１へ打ち込まれる。従って、ＬＯＣＯＳ酸化膜４と埋め込み酸化膜６がつながり、ＬＯＣＯＳ酸化膜４と埋め込み酸化膜６から構成される素子間分離領域が形成される。

【００３１】本実施例によれば、半導体素子が形成される個々の活性領域をＬＯＣＯＳ酸化膜４と埋め込み酸化膜６から成る素子間分離領域によって包囲し、電気的に完全に絶縁することができる。また、ＬＯＣＯＳ酸化膜４の膜厚を厚くする必要がないので、シリコン基板１の表面には、平坦性が良く幅の狭い素子間分離領域が形成できる。

【００３２】（実施例２）次に、本発明の一実施例である素子間分離領域およびその製造方法を図４～６を用いて説明する。

【００３３】本実施例の素子間分離領域は、図５または図６に示すように、個々の半導体素子領域が形成される単結晶シリコン層７を包囲した埋め込み酸化膜６によって構成されている。

【００３４】本実施例の素子間分離領域は、例えば、図４～図６に示す工程によって形成される。

【００３５】まず、図４に示すように、シリコン基板１の表面に熱酸化処理により酸化シリコン膜２を形成し、次いで、シリコン基板１の表面の素子間分離領域を必要とする位置に、台形のホトレジスト８によるマスクを形成する。

【００３６】次に、実施例１に記載した製造方法と同様に、シリコン基板１の全面に、ホトレジスト８を貫通しないエネルギー、例えば、１００～２００ＫｅＶで、酸素イオンを10^{17}～$10^{18}$$cm^{-2}$打ち込む。続いて、ホトレジスト８を除去した後、例えば、Ａｒ雰囲気中で１１００℃以上の高温アニールを約６時間行ない、図５に示すように、シリコン基板１の表面層に約0.１～1.０μmの単結晶シリコン層７を形成し、同時に、約0.４μmの埋め込み酸化膜６を形成する。この際、ホトレジスト８を貫通しないエネルギーで酸素イオンを打ち込んでいるので、ホトレジスト８の下方には、埋め込み酸化膜６は形成されない。しかし、ホトレジスト８の形状が台形であることから、ホトレジスト８の端部においては、酸素イオンがシリコン基板１へ打ち込まれ、形成された埋め込み酸化膜６がシリコン基板１の内部から表面方向へ曲がり、シリコン基板１の表面にまで達する。

【００３７】なお、個々の活性領域の電気的な絶縁を完全なものとするため、ホトレジスト８の寸法を短くして、図６に示すように、隣接する埋め込み酸化膜６をつなげてもよい。

【００３８】本実施例によれば、半導体素子が形成される個々の活性領域を埋め込み酸化膜６から成る素子間分離領域によって包囲し、電気的に完全に絶縁することができる。また、ＬＯＣＯＳ酸化膜４を併用しないため、シリコン基板１の表面には、平坦で幅の狭い素子間分離領域が形成できる。

【００３９】（実施例３）次に、本発明の一実施例である素子間分離領域およびその製造方法を図７および図８を用いて説明する。

【００４０】本実施例の素子間分離領域は、図８に示すように、ＬＯＣＯＳ酸化膜４および埋め込み酸化膜６によって構成されており、埋め込み酸化膜６がＬＯＣＯＳ酸化膜４の端部の下方において、シリコン基板１の表面方向へ曲がり、ＬＯＣＯＳ酸化膜４とつながっている。しかし、ＬＯＣＯＳ酸化膜４の端部は、活性領域である単結晶シリコン層７には形成されず、単結晶シリコン層７を包囲する埋め込み酸化膜６の外側に形成されている。

【００４１】まず、実施例２に記載した製造方法と同様に、図４に示したように、台形のホトレジスト８をマスクとして、シリコン基板１の全面にホトレジスト８を貫通しないエネルギーで、酸素イオンを打ち込み、続いて、ホトレジスト８を除去した後、高温アニールを行なうことにより、個々の単結晶シリコン層７を包囲する埋め込み酸化膜６を形成する。

【００４２】次に、図７に示すように、シリコン基板１上に窒化シリコン膜３をＣＶＤ法で堆積した後、ホトレジスト５をマスクにして、埋め込み酸化膜６によって包囲された隣接する単結晶シリコン層７の間に位置する窒化シリコン膜３をエッチングする。次に、ホトレジスト５を除去した後に、図８に示すように、選択酸化を行なうことにより、ＬＯＣＯＳ酸化膜４を形成する。

【００４３】本実施例によれば、半導体素子が形成される個々の活性領域をＬＯＣＯＳ酸化膜４と埋め込み酸化膜６から成る素子間分離領域によって包囲し、電気的に完全に絶縁することができる。また、活性領域にＬＯＣ

ＯＳ酸化膜４の端部が形成されないので、ＬＯＣＯＳ酸化膜４の端部で生じるリーク電流などによる半導体素子の特性劣化を防ぐことができる。

【００４４】以上、本発明者によってなされた発明を実施例に基づき具体的に説明したが、本発明は前記実施例に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【００４５】

【発明の効果】本願によって開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下の通りである。

【００４６】本発明によれば、半導体素子が形成される個々の活性領域を素子間分離領域で包囲して、電気的に完全に分離できるので、完全空乏型半導体素子が形成でき、半導体集積回路装置の高速化を可能とすることができる。また、平坦性が良く幅の狭い素子間分離領域を半導体基板の主面上に形成することができるので、微細加工が容易となり、半導体集積回路装置の高集積化を可能とすることができる。

【００４７】さらに、ＬＯＣＯＳ酸化膜またはホトレジストをマスクとして酸素イオンを半導体基板へ打ち込む簡単な製造工程によって、上記素子間分離領域を形成することができる。

【図面の簡単な説明】

【図１】本発明の一実施例である素子間分離領域を示す半導体基板の要部断面図である。

【図２】本発明の一実施例である素子間分離領域を示す半導体基板の要部断面図である。

【図３】本発明の一実施例である素子間分離領域を示す半導体基板の要部断面図である。

【図４】本発明の他の実施例である素子間分離領域を示す半導体基板の要部断面図である。

【図５】本発明の他の実施例である素子間分離領域を示す半導体基板の要部断面図である。

【図６】本発明の他の実施例である素子間分離領域を示す半導体基板の要部断面図である。

【図７】本発明の他の実施例である素子間分離領域を示す半導体基板の要部断面図である。

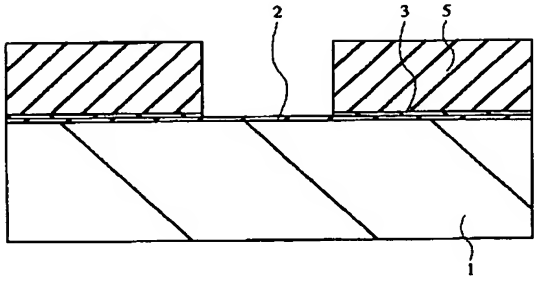
【図８】本発明の他の実施例である素子間分離領域を示す半導体基板の要部断面図である。

【符号の説明】

1　シリコン基板
2　酸化シリコン膜
3　窒化シリコン膜
4　ＬＯＣＯＳ酸化膜
5　ホトレジスト
6　埋め込み酸化膜
7　単結晶シリコン層
8　ホトレジスト

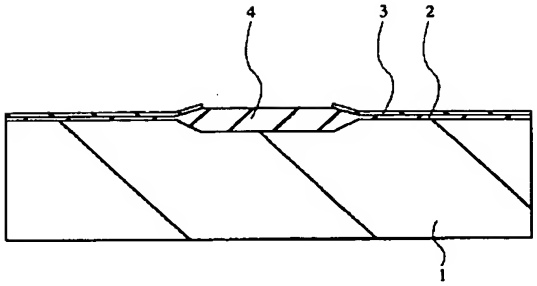
【図１】

図　1



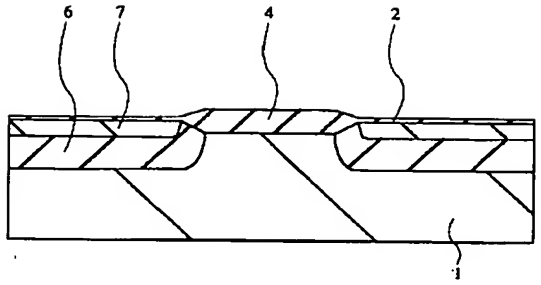
【図２】

図　2



【図３】

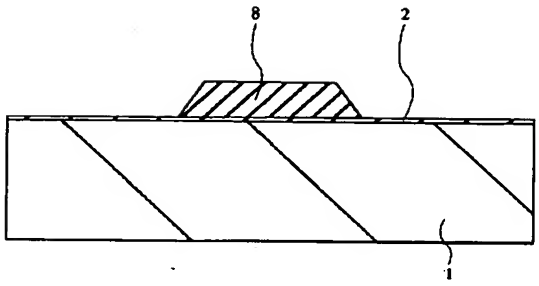
図　3



2：酸化シリコン膜
4：ＬＯＣＯＳ酸化膜
6：埋め込み酸化膜
7：単結晶シリコン層

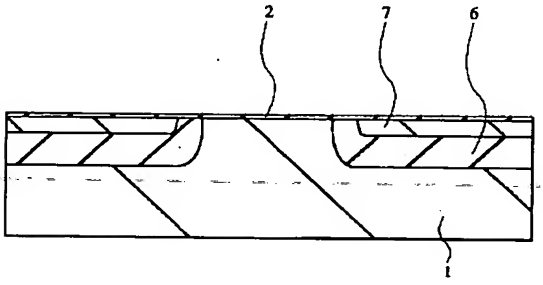
【図４】

図　4



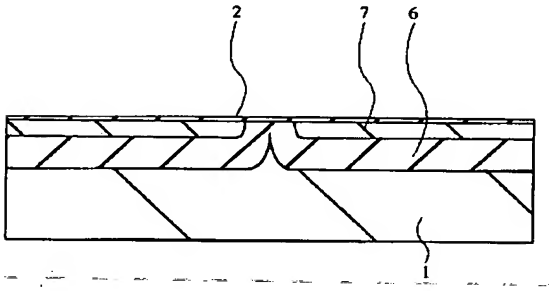
【図５】

図　5



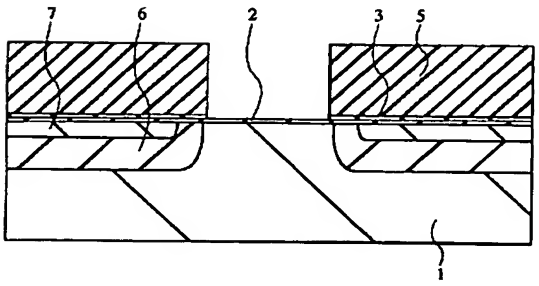
【図６】

図　6



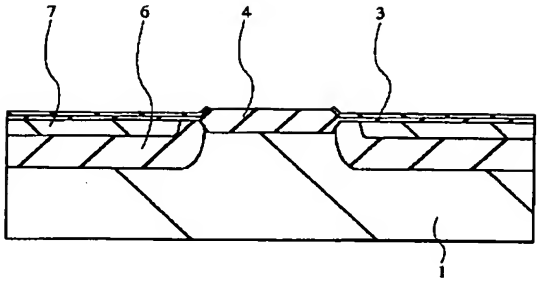
【図７】

図　7



【図８】

図　8



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